What is claimed is:

1. A method for determining a plurality of clock delay values, each delay value associated with a delay element on a clock line leading to a clock sink in a synchronous circuit, the method comprising:

determining an initial set of delay values; and

executing an optimization algorithm, beginning with the initial set of delay values, to arrive at a set of delay values that at least approximately meet a criteria while satisfying timing constraints associated with selected pairs of logically connected clock sinks, wherein the optimization algorithm comprises randomly modifying the set of delay values.

2. The method of claim 1 wherein the determining step comprises:

randomly selecting the initial set of delay values.

3. The method of claim 1 wherein the determining step comprises:

executing a linear programming algorithm to determine the initial set of delay values.

4. The method of claim 1 wherein the determining step comprises:

executing a quadratic programming algorithm to determine the initial set of delay values.

5. The method of claim 1 wherein the optimization algorithm is a genetic algorithm.

6. The method of claim 5 wherein determining step comprises:

determining multiple initial sets of delay values;

7. The method of claim 5 wherein the genetic algorithm comprises the following steps:

selecting parent sets of delay values;

crossing over so as to produce a child set of delay values;

mutating the child set of delay values;

evaluating how well the child set of delay values meets the criteria; and

conditionally discarding the child set on the basis of the evaluating step.

8. The method of claim 7 wherein the selecting step comprises:

conducting a random tournament.

9. The method of claim 7 wherein the crossing over step comprises:

dividing two parents into corresponding regions, wherein the number and locations of the regions are random; and

randomly swapping corresponding regions of the parents, so as to result in two region-by-region swapped set of delay values that are children.

10. The method of claim 7 wherein the mutating step comprises:

adding to each delay value in the child set of delay values a Gaussian random variable having zero mean and a predetermined variance.

11. The method of claim 7 wherein the evaluating step comprises:

calculating an objective function for the child set; and

determining whether the child set satisfies the timing constraints.

12. The method of claim 7 further comprising:

iteratively repeating the selecting, crossing over, mutating, evaluating and conditionally discarding steps.

13. The method of claim 1 wherein the optimization algorithm is a gradient search algorithm.

14. The method of claim 13 wherein the gradient descent algorithm comprises the following steps:

perturbing a set of delay values;

evaluating how well the perturbed set of delay values meets the criteria; and

conditionally discarding the perturbed set on the basis of the evaluating step.

15. The method of claim 14 further comprising:

iteratively repeating the perturbing, evaluating and conditionally discarding steps; and

if the perturbed set is not discarded, then adjusting the values of the perturbed set in the same direction relative to the corresponding values in the initial set.

16. The method of claim 14 wherein the perturbing step comprises

randomly perturbing the initial set of values.

17. The method of claim 1 wherein the timing constraints are defined substantially as follows:

$$T_S + C_i + G_i + D_{ijL} < T_{CLK+} + C_j + G_j$$

$$C_i + G_i + D_{ijS} > C_j + G_j + T_H$$

where T_S is the setup time, T_H is the hold time, D_{ijL} is the longest propagation delay between a pair of logically connected clock sinks i and j, D_{ijS} is the shortest propagation delay between a pair of logically connected clock sinks i and j, C_i and C_j measure relative clock skew between the sinks i and j, and G_i and G_j are the delay values for the sinks i and j out of the set of delay values.

18. The method of claim 17 wherein the criteria is minimization of a quantity selected from the group consisting of a quantity related to a clock frequency, a quantity related to a sum of the set of delay values, and a quantity related to the distances of the delay values from a target.

19. A synchronous circuit comprising:

a plurality of clock sinks;

a plurality of clock delay elements connected to the clock sinks, each clock delay element having a delay value, wherein the delay values are set according to a method comprising a step of determining initial values for the delay values and a step of executing an optimization algorithm, beginning with the initial set of delay values, to arrive at a set of delay values that at least approximately meet a criteria while satisfying timing constraints associated with selected pairs of logically connected clock sinks, wherein the optimization algorithm comprises randomly modifying the set of delay values.

20. A computer readable medium on which is embedded computer software, the software comprising a program, the program performing a method for determining a plurality of clock delay values, each delay value associated with a delay element on a clock line leading to a clock sink in a synchronous circuit, the method comprising:

determining an initial set of delay values; and

executing an optimization algorithm, beginning with the initial set of delay values, to arrive at a set of delay values that at least approximately meet a criteria while satisfying timing constraints associated with selected pairs of logically connected clock sinks, wherein the optimization algorithm comprises randomly modifying the set of delay values.